

Digital Electronics

(USIT102)

F. Y. B. Sc. (Information Technology)
Semester I
(Mumbai University)

Strictly as per the New Revised Syllabus of
Mumbai University w.e.f. academic year 2016-2017

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J. S. Katre

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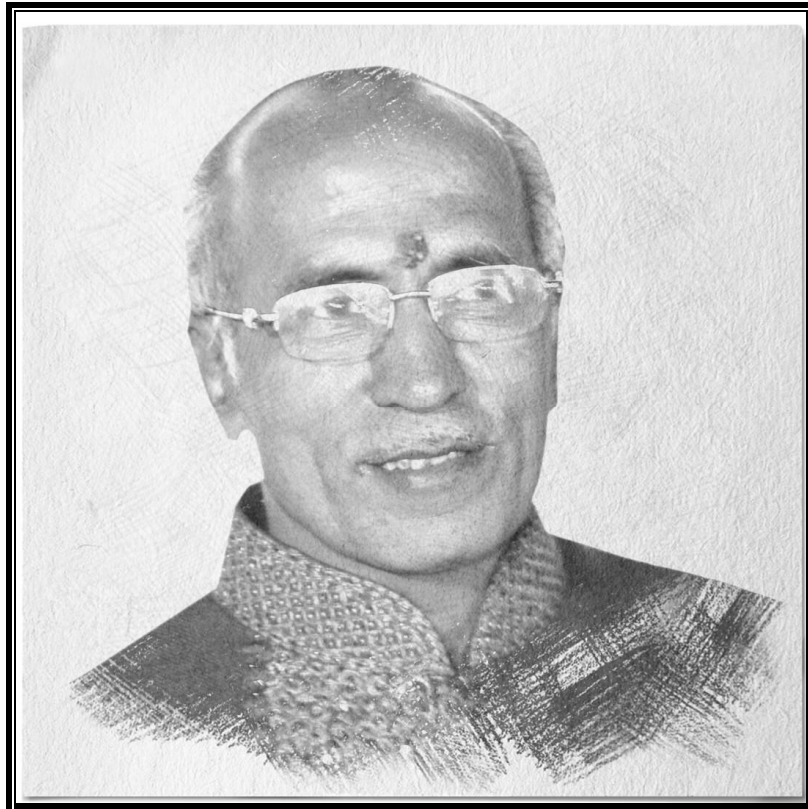
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*We dedicate this Publication soulfully and wholeheartedly,
in loving memory of our beloved founder director,
Late Shri. Pradeepji Lalchandji Lunawat,
who will always be an inspiration, a positive force and strong support
behind us.*



“My work is my prayer to God”

- Lt. Shri. Pradeepji L. Lunawat

*Soulful Tribute and Gratitude for all Your
Sacrifices, Hardwork, and 40 years of Strong Vision...*

Syllabus...

Digital Electronics : Sem. I, (Information Technology (MU-BSc))

Unit I

Number System :

Analog System, digital system, numbering system, binary number system, octal number system, hexadecimal number system, conversion from one number system to another, floating point numbers, weighted codes binary coded decimal, non-weighted codes, Excess – 3 code, Gray code, Alphanumeric codes – ASCII Code, EBCDIC, ISCII Code, Hollerith Code, Morse Code, Teletypewriter (TTY), Error detection and correction, Universal Product Code, Code conversion. **(Refer chapters 1 and 2)**

Binary Arithmetic :

Binary addition, Binary subtraction, Negative number representation, Subtraction using 1's complement and 2's complement, Binary multiplication and division, Arithmetic in octal number system, Arithmetic in hexadecimal number system, BCD and Excess – 3 arithmetic. **(Refer chapter 3)**

Unit II

Boolean Algebra and Logic Gates :

Introduction, Logic (AND OR NOT), Boolean theorems, Boolean Laws, De Morgan's Theorem, Perfect Induction, Reduction of Logic expression using Boolean Algebra, Deriving Boolean expression from given circuit, exclusive OR and Exclusive NOR gates, Universal Logic gates, Implementation of other gates using universal gates, Input bubbled logic, Assertion level. **(Refer chapter 4)**

Minterm, Maxterm and Karnaugh Maps :

Introduction, minterms and sum of minterm form, maxterm and Product of maxterm form, Reduction technique using Karnaugh maps – 2/3/4/5/6 variable K-maps, Grouping of variables in K-maps, K-maps for product of sum form, minimize Boolean expression using K-map and obtain K-map from Boolean expression, Quine Mc Cluskey Method. **(Refer chapter 5)**

Unit III

Combinational Logic Circuits :

Introduction, Multi-input, multi-output Combinational circuits, Code converters design and implementations.

Arithmetic Circuits :

Introduction, Adder, BCD Adder, Excess – 3 Adder, Binary Subtractors, BCD Subtractor, Multiplier, Comparator. **(Refer chapter 6)**

Unit IV

Multiplexer, Demultiplexer, ALU, Encoder and Decoder :

Introduction, Multiplexer, Demultiplexer, Decoder, ALU, Encoders. **(Refer chapter 7)**

Sequential Circuits : Flip-Flop :

Introduction, Terminologies used, S-R flip-flop, D flip-flop, JK flip-flop, Race-around condition, Master – slave JK flip-flop, T flip-flop, conversion from one type of flip-flop to another, Application of flip-flops. **(Refer chapter 8)**

Unit V

Counters :

Introduction, Asynchronous counter, Terms related to counters, IC 7493 (4-bit binary counter), Synchronous counter, Bushing, Type T Design, Type JK Design, Presettable counter, IC 7490, IC 7492, Synchronous counter ICs, Analysis of counter circuits. **(Refer chapter 9)**

Shift Register :

Introduction, parallel and shift registers, serial shifting, serial-in serial-out, serial-in parallel-out , parallel-in parallel-out, Ring counter, Johnson counter, Applications of shift registers, Pseudo-random binary sequence generator, IC7495, Seven Segment displays, analysis of shift counters. **(Refer chapter 10)**

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**Unit I****Chapter 1 : Number Systems 1-1 to 1-22**

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Unit I

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Arithmetic Circuits : Introduction, Adder, BCD Adder, Excess – 3 Adder, Binary Subtractors, BCD Subtractor, Multiplier, Comparator.

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Unit IV

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Unit IV

Chapter 8 : Flip Flops 8-1 to 8-29

Syllabus : Sequential Circuits : Flip-Flop : Introduction, Terminologies used, S-R Flip-Flop, D Flip-Flop JK Flip-Flop, Race-around condition. Master slave JK flip-flop, T flip-flop, Conversion from one type of flip-flop to another, Application of flip-flops.

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Unit V

Chapter 10 : Shift Registers 10-1 to 10-16

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